Microwave performances dependence on geometry for Graphene Field Effect Transistors (GFETs)

M. A. Giambra*, L. Zeiss, A. Benfante, E. Calandra, S. Stivala, A. Busacca
DEIM, University of Palermo, Viale delle Scienze, Ed. 9, 90128 Palermo, Italy

W. H. P. Pernice, R. Danneau
Institute of Nanotechnology (INT), Karlsruhe Institute of Technology (KIT),
76344 Eggenstein-Leopoldshafen, Germany

*marcoangelo.giambra@unipa.it

Abstract

Graphene is a relatively new material whose unique properties have attracted significant interest for its use in electronic and photonic applications [1-2]. In particular, the field effect has been proved in graphene samples and this feature, together with the high carrier mobility observed, makes graphene an interesting solution for the realization of electronic devices operating in the microwave range.

In our work, we performed an experimental investigation on a number of Graphene Field Effect Transistors (GFETs) purposely built in order to evaluate the dependence of microwave performances as function of device geometry. More precisely, we studied the behavior of the cut-off frequency (f_t) and of the output impedance (Z_{out}) when both the gate-drain/gate-source distance (Δ) and the gate length (L_g) are varied (Fig. 1). In order to perform the abovementioned analysis in a statistically meaningful way, we fabricated 24 GFETs families on the same chip (330μm thick sapphire [3], with gold metal layers and palladium pads). Each family comprises 10 devices with the same Δ and L_g values.

After fabrication, the GFETs were characterized in both DC and RF regimes. DC measurements allowed us to obtain the static transconductance curves (I_d vs V_{gs}) and, hence, to evaluate the incremental low-frequency transconductance (g_m), whose value deeply influences the device cut-off frequency. The scattering parameters were then measured, in the region where g_m exhibits its highest value, by using a vector network analyzer. The de-embedding of the devices was performed through modeling of the coplanar launching structures, by combined use of EM simulations and experimental measurements on auxiliary test structures (open, short and thru-line) implemented on the same chip. This procedure allowed us to evaluate the short circuit current gain (h_{21}), f_t and Z_{out} of the intrinsic device alone.

As example of results achieved, Fig. 2 illustrates the behavior of f_t and Z_{out} as a function of the device geometrical parameters.

References

[1] F. Schwierz, *Nat Nano*, **vol. 5**, **no. 7** (2010), pp. 487–496.

[2] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, *Nat. Nanotechnol.*, **vol. 9** (2014), pp. 768–779.

[3] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, *J. Phys. Chem. B*, **vol. 108**, **no. 52** (2004), pp. 19912–19916.

Figures

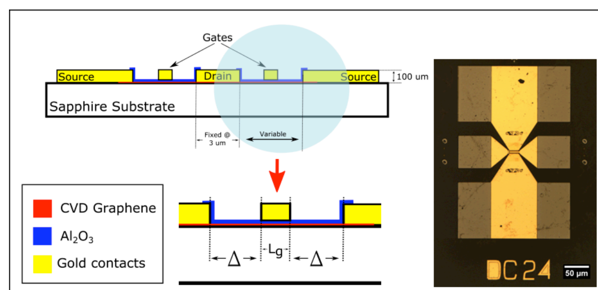

Fig. 1: GFETs cross section (left) and photo (right) of the fabricated device

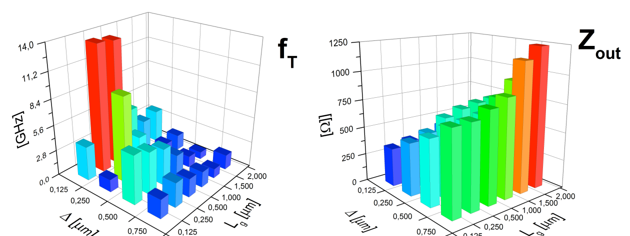

Fig. 2: Dependence of f_T (left) and Z_{out} (right) on device geometrical parameters.